HB-DAC1704 Board
Version V2.0

1. Introduction

Why a new DAC design? There are some good reasons for designing this new DAC:

Jitter: It is well known that jitter reduces the sound quality. Jitter can be generated everywhere, but there are some major jitter sources you can find when looking at the audio chain: the first source is the CD player itself. You can buy a better one with good mechanics, but the electronics of the player adds some jitter, too. Normally, digital audio will then be transported via the SPDIF, AES/EBU or USB to the digital receiver. These standards are defined to contain data and clock on one wire (differential or coaxial) and the receiver has the job to split the clock from the data. Also the best chips add a lot of jitter by doing this. Less then about 200ps additional jitter is not possible. The only way to overcome this problem is to resynchronize the incoming clock with a clean jitter free synchronous clock.

There are several possibilities to generate a synchronous clock. You could take a quite complex PLL design. Complex because a PLL normally add a lot of jitter like the PLL in the digital receiver does for clock recovery. You could add a VCXO (voltage controlled crystal oscillator) but this would increase costs and complexity and then you have the problem to be fixed on one sample rate. Another method is to take a sample rate converter (SRC) with a fixed output frequency which is generated by a low jitter oscillator. The input frequency is variable. This means the sample rate is variable (here from 44.1 kHz to 192 kHz) which is a big advantage. This concept reduces the jitter nearly to the jitter of the oscillator plus the jitter of the output stage of the SRC. If you add a resynchronisation after the SRC you could improve the jitter once again. Here this is done by Flip Flops which are clocked with the crystal oscillator.

Digital filtering: For easy analogue filtering normally an 8 times oversampling filter is used. But these filters add pre- and post ringing to signal. The sound is not so precise and clear. It is slushier. In the HB-DAC1704 no traditional oversampling filters are used. The upsampling method is done by a very precise interpolation in the SRC and no downsampling filtering is needed when using the direct downsampling feature of the new high end chip (SRC4392) from Texas Instruments.
To verify the difference between an SRC as “oversampling filter” and a direct audio chain without any digital filtering the design includes a mode called NON oversampling mode (NOS). Here the clock is taken from the digital receiver to clock the DACs directly. The NOS mode in I2S is not possible.

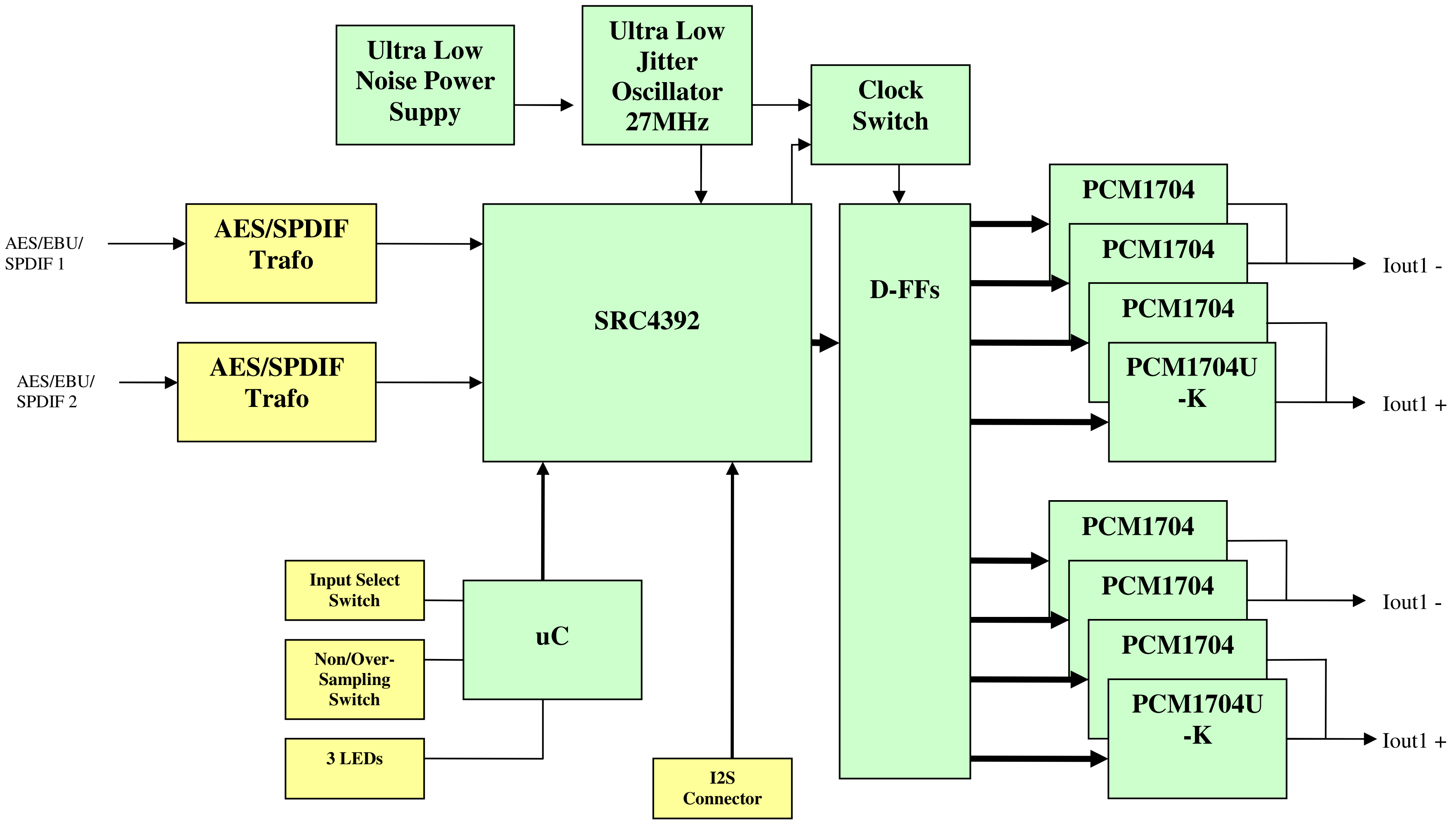
DAC: Here the very best R2R DAC is used (PCM1704). The advantage of a R2R DAC versus the sigma delta DAC is a much better resolution of small signals. And this is the most common case with audio to have excellent music quality when the music is more silent and more complex instead of loud where the ears distortion is growing and effects like sound masking occurs. In the HB-DAC1704 four DACs per channel are used to reduce noise and THD. They can work in parallel or in balanced mode. The balanced mode gives a better noise immunity (common mode rejection).

In total these advantages create a very precise and clear sound.

Other features included are the two AES/EBU/SPDIF balanced inputs isolated with a transformer and selectable ground connection and an I2S input.

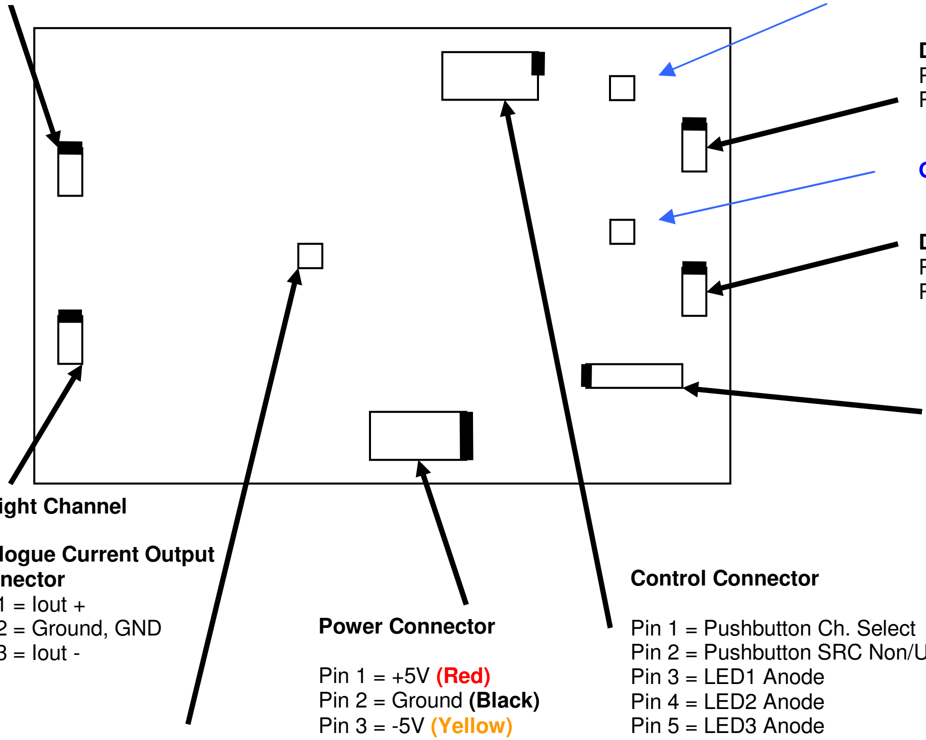
The intention of missing IV/ converter/post analogue filtering is that everybody can build up his own I/V converter and analogue filters with his own goals of realizing ultimate audio quality. A very low noise power supply/regulator delivering +/-5V at 200mA is needed for the HB-DAC1704. It should have low noise in the lower frequency range (<1kHz). Borbely Audio offers very high quality I/V converters/filters and power supplies/regulators. The discrete JFET/FET amplifiers offer very high resolution also with small amplitudes the DACs have.

2. Block Diagram



3. How to connect to the board

= Pin1



Left Channel

Right Channel

Ground Jumper AES/EBU/SPDIF 1

Digital Connector 1
Pin 1 = AES/EBU/SPDIF Trafo postive
Pin 2 = AES/EBU/SPDIF Trafo negative

Ground Jumper SPDF2

Digital Connector 2
Pin 1 = AES/EBU/SPDIF Trafo postive
Pin 2 = AES/EBU/SPDIF Trafo negative

I2S Connector

Pin 1 = Bit clock
Pin 2 = Word Sync
Pin 3 = Data In
Pin 4 =GND
Pin 5 = do not connect

Analogue Current Output Connector
Pin 1 = Iout +
Pin 2 = Ground, GND
Pin 3 = Iout -

Power Connector

Pin 1 = +5V **(Red)**
Pin 2 = Ground **(Black)**
Pin 3 = -5V **(Yellow)**

Control Connector

Pin 1 = Pushbutton Ch. Select (PB1)
Pin 2 = Pushbutton SRC Non/Upsampling (PB2)
Pin 3 = LED1 Anode
Pin 4 = LED2 Anode
Pin 5 = LED3 Anode
Pin 6 = for future use (do not connect)
Pin 7 = LED4 Anode
Pin 8 = Ground
Pin 9 = Ground
Pin 10 = for future use (do not connect)

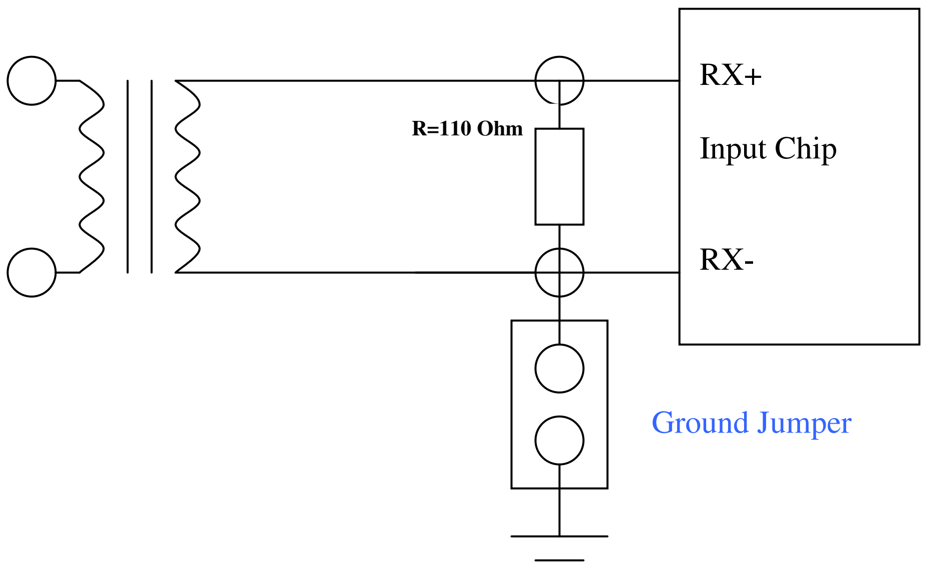
Data Inversion Jumper
Jumper assembled = Output Con. Pin 3 = Iout – (balanced mode)
Jumper NOT assembled = Output Con. Pin 3 = Iout + (parallel mode)

3.1 Power

The board is delivered with a power connector with coloured cables. **Connect RED to +5V, YELLOW to -5V and BLACK to Ground.** The board will be destroyed if you connect it wrong. (It is not possible to plug in the connector in a wrong way). Be sure that the voltages are in the specified range (+/-5V, +/-5%). No guarantee for reversed power connections!

3.2 AES/EBU/SPDIF Inputs

The digital audio receiver offers balanced inputs RX+ and RX-. The two AES/EBU/SPDIF inputs have signal isolation transformers. After the transformers the user has the possibility for grounding the RX-Input. Then the Ground Jumper AES/EBU should be assembled (default: assembled). For SPDIF the Jumper should be set. Figure 4 shows the simplified input schematic for AES/EBU/SPDIF. The AES/EBU input is terminated with 110 Ohm while SPDIF is terminated with 75 Ohm. Please order your wanted impedance for each input (75 Ohm or 110 Ohm).



3.2 I²S Input

The I²S input is a low voltage (3.3V) digital input.

3.3 Analogue Out

User can choose between balanced current output or parallel output of the four DAC chips per channel. With **Data Inversion Jumper** assembled both channels are in balanced mode. Pin 3 of the connectors are inverted (I out -). Without jumper the two DAC chips are working in parallel. User must then connect Pin 1 and Pin 3 together.

3.4 Control Interface

To control the board user can connect two pushbuttons and 4 LEDs. See chapter 4 for function description. Connect the second pins of the pushbuttons with ground (pin 8,9). The anodes of the LEDs must be connected to the connector pins, the cathodes to ground (pin 8,9).

4. Functional Description

Most of the functionality is explained in the introduction and can be studied in the block diagram. It should be noted that the microcontroller (uC) is normally in total power down mode. No asynchronous clock from the uC disturbs the signals. The DACs power supplies are decoupled with low ESR ceramic and high quality electrolytic (Rubycon) capacitors with more than four times the value as specified in the datasheet. The critical oscillator is a special very low jitter oscillator and has its own discrete power supply to further reduce the jitter.

The PCB is a 4 layer design to improve digital impedance requirements and to reduce the overall noise and crosstalk. See the noise specs at the end of this manual.

4.1 uC Functionality

The main function of the uC is to initialize the SRC4392, to select the different inputs and to display the selected functions.

4.1.1 Function Select

With two pushbuttons the user can select:

- Channel Select (PB1). Every push on the button changes the input channel. The default (PB1 not pressed) is the AES/EBU/SPDIF channel 1, followed by AES/EBU/SPDIF channel 2 and I²S channel. Then it starts again with the AES/EBU/SPDIF channel 1.
- Non/Oversampling mode. Every push on the button toggles between non oversampling and “oversampling” mode.

4.1.2. LED Indication

Four LEDs indicates the board status.

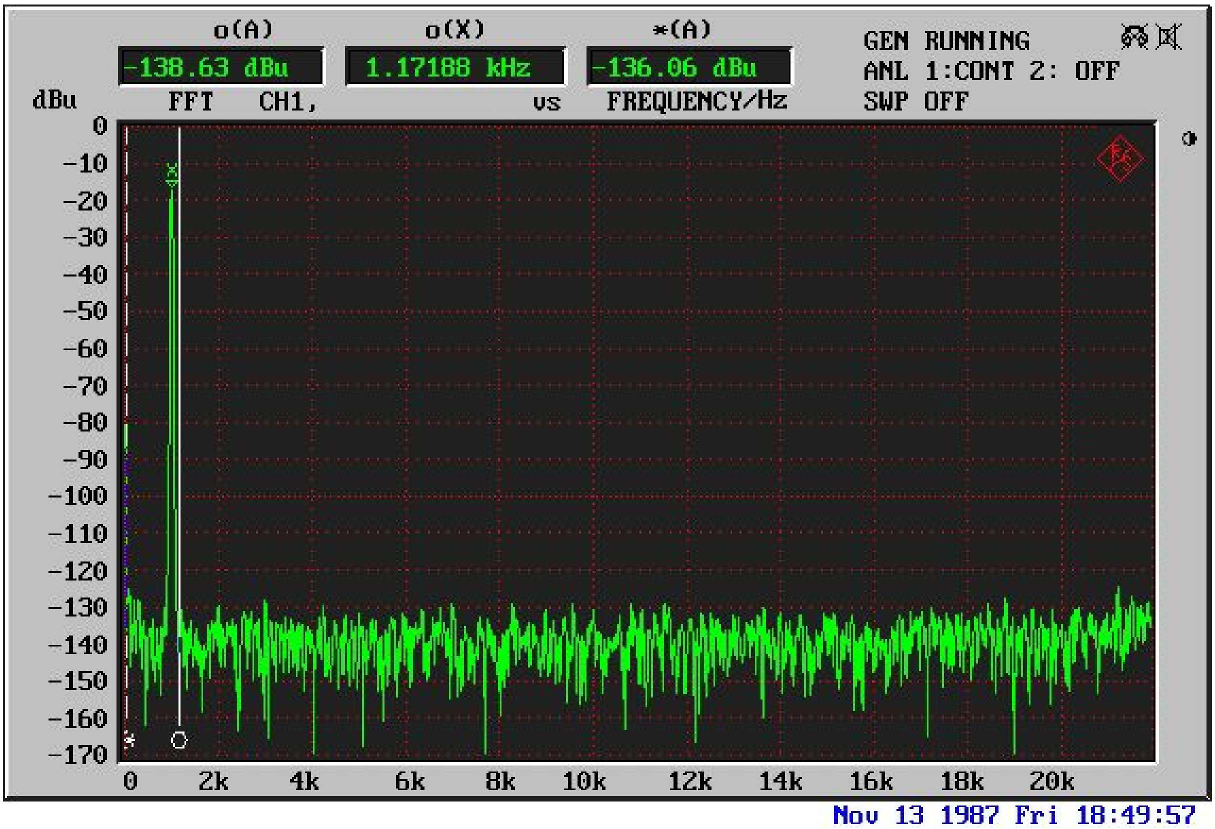
LED1 on:	AES/EBU/SPDIF channel 1 selected
LED2 on:	AES/EBU/SPDIF channel 2 selected
LED3 on:	I²S channel selected
LED4 on:	Non oversampling NOS mode selected, LED4 off: normal OS mode via SRC

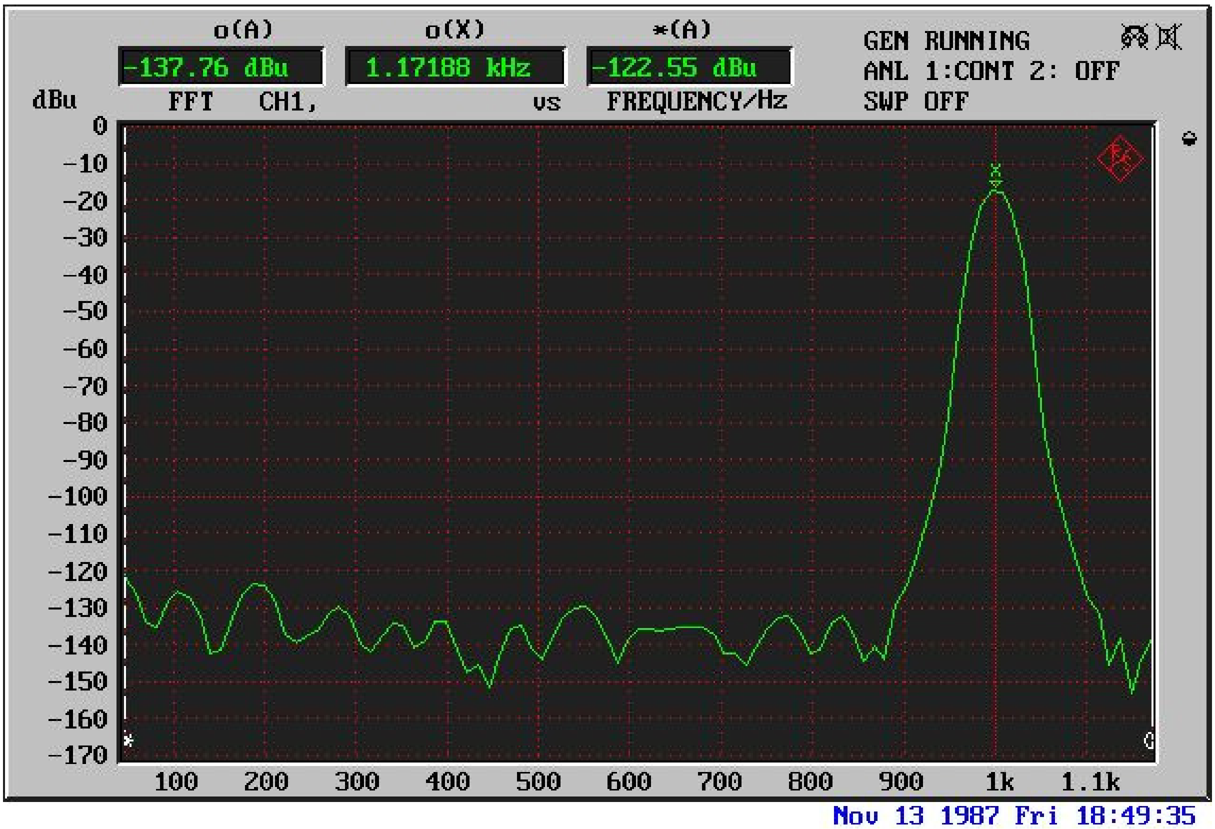
5. Characteristics of HB-DAC1704 Board Version V2.0

• PCB:	Version V2.0, 4 Layer, Dimensions: 64.8 mm x 88 mm
• Supply voltage(s):	+/-5V +/-5% regulated, low noise supply required
• Supply current:	typ. 180mA for +5V, typ. 240mA for -5V
• Inputs:	2 x AES/EBU/SPDIF input, 110/75 Ohm isolated with signal transformer 1 x I^2S input (header)
• Outputs analogue:	4 x Current outputs, max. 2.4 mA/output in balanced mode or 4.8mA/output in parallel mode, Stereo, each Channel with 4 DACs in parallel or in balanced mode. Selectable with Jumper.
• Control Interface:	LED current to ground: 22mA max. , short circuit protected
• Input Sample Rate:	4 kHz to 210.9 kHz
• DAC Sample Clock:	210.9kHz, or input clock rate w/o sample rate converter (selectable)
• System Clock:	27MHz, Period Jitter nominal 0.5ps rms
• Micro Controller:	always in total power down, except by channel selection or during init
• THD:	PCM1704UK: 0.0008%
• Noise:	Depends on the noise of the power supply (>120dB, typ.)

6. Measurements

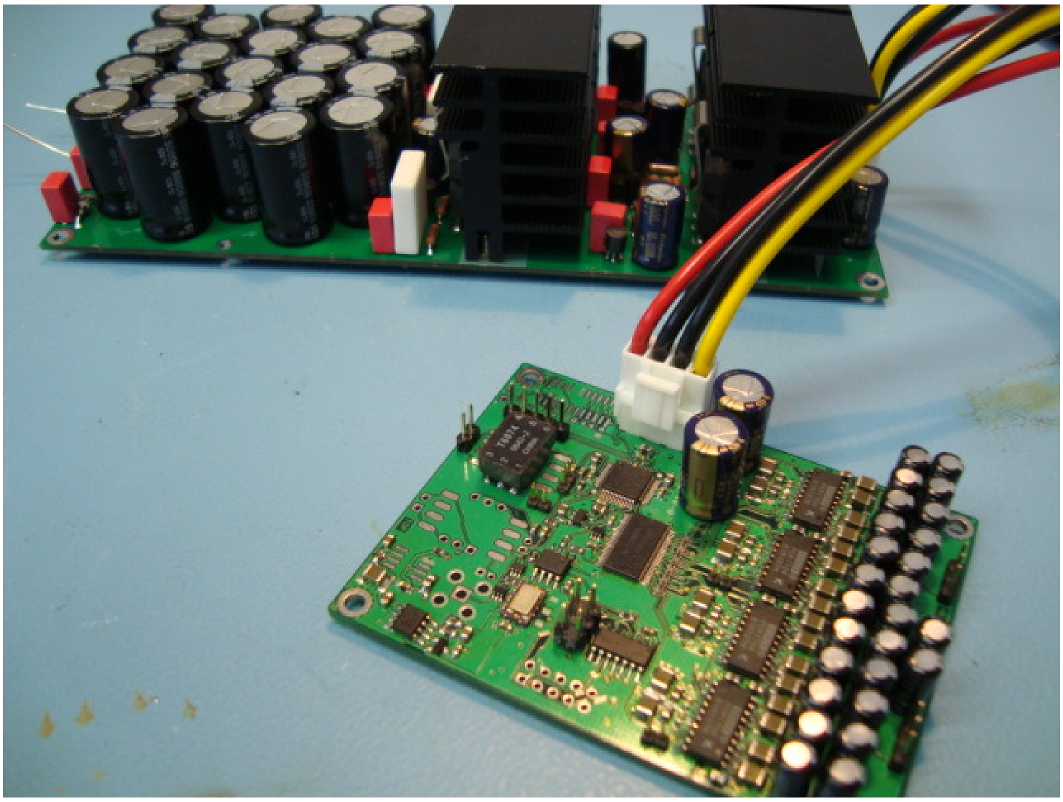
FFT (0Hz..22kHz and 0Hz..1.1kHz) measured with R&S UPL Audio Analyser, unweighted (no filter), passive I/V conversion in balanced mode with two 39 Ohm resistors with shunt regulated +/-5V power supply

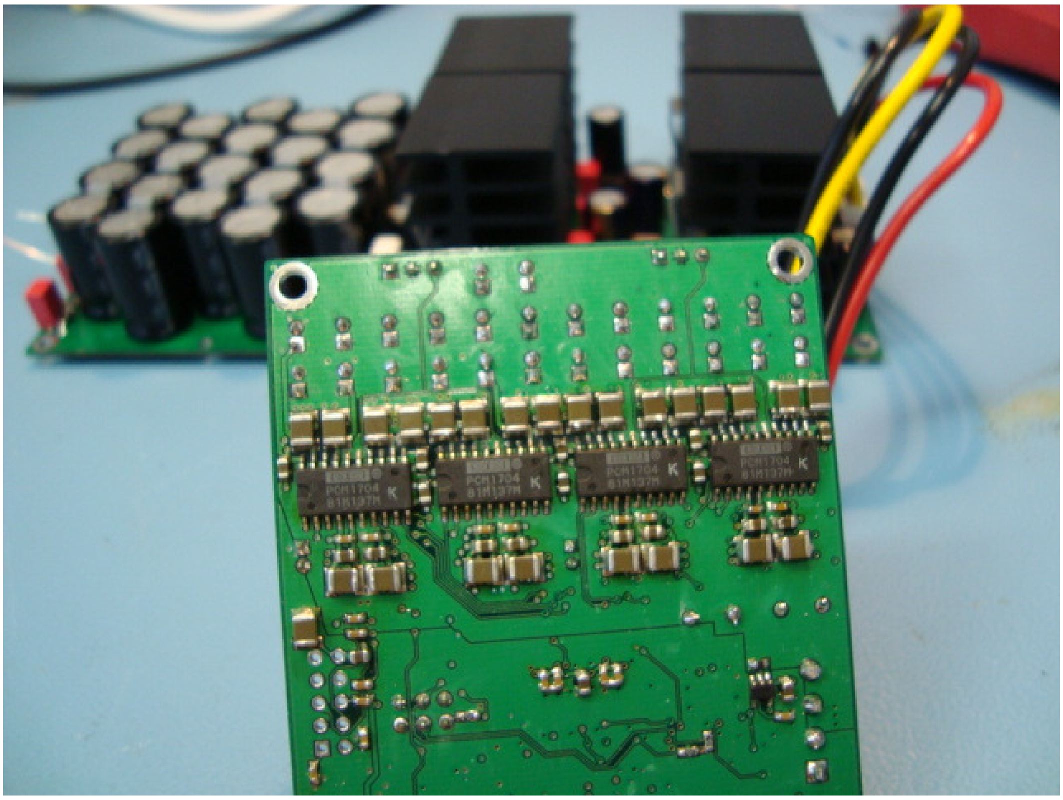




7. Photos

Two photos are shown from the first prototype with only one SPDIF input and control header not assembled. The first is the top the second the bottom side. Also the shunt regulator can be seen with 20 Rubycon input capacitors with a total capacitance of 47000uF each voltage.





8. Dimensions of Mounting Holes